## REMARKS

Claims 48-65 are pending in the application and all stand finally rejected. In addition, the drawings and specification stand objected to. Reconsideration and withdrawal of the pending rejections and objections is respectfully requested.

Rejections under 35 U.S.C. § 103(a)

Claims 48-65 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over United States patent number 5,346,838 to Ueno (Ueno) in View of United States Patent Number 4,861,731 to Bhagat (Bhagat).

The present invention relates to a planar SRAM cell using bipolar latch-up and gated diode breakdown. Claim 48 recites:

> A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising the following steps: providing a semiconductor substrate; providing doped silicon regions to form a multi-region planar thyristor having at least four regions; forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode; connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor; and incorporating said multi-region planar thyristor in a memory device. (Emphasis added).

As previously discussed in the amendment filed on February 26, 2003, Ueno and Bhagat, taken alone or in combination, do not teach or suggest "incorporating said multi-region planar thyristor in a memory device," as claimed. The now-pending Office Action states that "the thyristor of the present claims is disclosed as the memory device" and asserts that, "[s]ince the thyristor is the memory device, the step of 'incorporating' the thyristor 'in a memory device' can only be interpreted that the thyristor is intended to be

used as a memory device," (emphasis added). The thyristor, however, is not the memory device of claim 48. Therefore, the logic of the proposition fails and the step of incorporating the thyristor is not an intended use.

The application discloses that the "invention provides... static memory cells and memory arrays by the use of parasitic bipolar transistors which can be latched in a bistable on state with small area transistors. Each bipolar transistor memory cell includes a gate which is pulse biased during the write operation to latch-up the cell." Column 2, lines 50-55. The specification thus teaches the thyristor as a portion of a memory device. Furthermore, there is nothing in the specification that tends to limit the memory device to being the thyristor. Therefore it is clear that the thyristor is not the "memory device" of claim 48, and the step of incorporating the thyristor is not an "intended use." Rather, the step of "incorporating said multi-region planar thyristor in a memory device" is a valid process step.

The Office Action states that "Ueno discloses in figures 3,4, and 6a mutually coupling at least two gates of the plurality of gates to a write row address line of the memory integrated circuit." Ueno does not, however, teach or suggest a memory integrated circuit. The Ueno reference is directed to "a method for fabricating an insulated gate control thyristor." According to Ueno: "FIG. 3 is a cross-sectional view showing a unit structure of the first embodiment: a real insulated gate control thyristor whose current capacity is on the order of several tens of Amperes includes a plurality of the unit structures which are repeated in the lateral directions in FIG. 3, and which are connected in parallel fashion,"(emphasis added). Column 7, lines 23-28.

There in nothing in Fig. 3, or in figures 4 and 6a to teach or suggest a memory device. Nor, as previously noted, is there anything in Ueno and Bhagat, taken alone or in combination, to teach or suggest "incorporating said multi-region planar thyristor in a memory device ." Accordingly, Ueno and Bhagat do not anticipate claim 48 or render it obvious and the rejection of claim 48 under 35 U.S.C. § 103(a) should be withdrawn.

Claims 49-54 each depend, directly or indirectly, from claim 48 and incorporate every limitation thereof. Therefore, the rejection of claims 49-54 under 35 U.S.C. § 103(a) should be withdrawn for at least the reasons given above in relation to claim 48.

Applicant reserves the right to contest the propriety of the proposed combination of Ueno and Bhagat at a future time.

Like claim 48, claim 55 includes the limitation of "incorporating said multi-region planar thyristor in a memory device." Therefore, the rejection of claim 55 under 35 U.S.C. § 103(a) should be withdrawn for at least the reasons given above in relation to claim 48.

Claims 56-61 each depend, directly or indirectly, from claim 55 and incorporate every limitation thereof. Therefore, the rejection of claims 56-61 under 35 U.S.C. § 103(a) should be withdrawn for at least the reasons given above in relation to claim 55.

Claim 62 includes the limitation of "connecting said at least one polysilicon gate to... a write row address line of a memory integrated circuit." Ueno and Bhagat are not related to memory devices and, taken alone or in combination, do not teach or suggest at least this feature of the claimed invention. Accordingly, the proposed combination of Ueno and Bhagat does not anticipate claim 62 or render it obvious, and the rejection of claim 62 under 35 U.S.C. § 103(a) should be withdrawn. For the same reasons, the rejections of claims 63-65 under 35 U.S.C. § 103(a) should also be withdrawn.

Rejections under 35 U.S.C. § 112, First Paragraph

Claims 62-65 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter not described in the specification. Claim 62 has been amended to more clearly define invention.

In relation to claim 62, the claim terminology "connecting said at least one polysilicon gate to said source for producing latch-up in said multi-region planar thyristor through a write row address line on a memory integrated circuit," (emphasis added) is supported in the specification in view of figures 10 and 6. Figure 10 shows a gate connected to a write row address line 34. Figure 6 shows a gate connected to a positive gate voltage. Accordingly the specification contains antecedent basis for the claim limitation of "connecting said at least one polysilicon gate to said source for producing latch-up in said multi-region planar thyristor through a write row address line on a memory integrated circuit." Therefore, claim 62 is fully supported by the specification and the rejection claim 62 under 35 U.S.C. § 112, first paragraph, is overcome.

In relation to claim 63, support for "forming a plurality of channels disposed between said thyristor structures" is found in figure 1, in which the channels are clearly shown, and in the specification: "[p]lanar transistor pairs or devices, noted generally 12, are separated from each other by isolation trenches 16, 18." Column 4, lines 11-13. Accordingly, the rejection of claim 63 under 35 U.S.C. § 112, first paragraph, should be withdrawn.

In relation to claim 64 the specification and figures provide antecedent basis for all claim limitations. Claim 64 includes the limitations of "connecting said at least one polysilicon gate to a voltage source," and "coupling said at least one polysilicon gate to a write row address line of said memory device." As discussed above in relation to claim 62, figure 10 shows a gate connected to a write row address line 34 and figure 6 shows a gate connected to a positive gate voltage. Together, figures 6 and 10 show a voltage connected to an electrical node including the gate and the write row address line 34. Accordingly, the specification provides the requisite antecedent basis for claim 64. Therefore, the rejection of claim 64 under 35 U.S.C. § 112, first paragraph, should be withdrawn. The rejection of claim 65 under 35 U.S.C. § 112, first paragraph, should be withdrawn for the same reasons as those given above in relation to claim 64.

Rejections under 35 U.S.C. § 112, Second Paragraph

Claims 48-62, 64 and 65 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The rejection of claims 48 and 55 relies on the premise that "incorporating said multi-region thyristor in a memory device" is an "intended use limitation." The foregoing discussion in relation to the rejection of claims 48 and 55 under 35 U.S.C. § 103(a) demonstrates, however, that the subject limitation is a structural limitation and not an intended use limitation. Accordingly, the rejection of claims 48 and 55 under 35 U.S.C. § 112, second paragraph, should be withdrawn.

In relation to claims 55 and 62, the Office Action asserts that claim element "for producing latch-up in said multi-region planar thyristor" constitutes an "intended use recitation." To the contrary, however, one of skill he art would understand that the subject claim element characterizes the gate structure, inasmuch as the gate is adapted to receive a particular voltage or range of voltages described by the claim element. Accordingly, "for producing latch-up in said multi-region planar thyristor" is not an "intended use recitation." Therefore, the rejection of claim 55 under 35 U.S.C. § 112, second paragraph should be withdrawn.

The claim 62 claim limitation "said thyristor is adapted to transition from a first one to a second one of said at least two possible current states," is believed to be a valid claim limitation. In addressing the use of "adapted to" in patent claims, the court has noted that "[r]ather than being a mere direction of activities to take place in the future, this language imparts a structural limitation..." In re Venezia 189 USPQ 149 (CCPA, 1976). Accordingly, the rejection of claim 62 under 35 U.S.C. § 112, second paragraph, is also believed to be overcome.

Objections to Drawings and Specification

The drawings stand objected to under 37 C.F.R. 1.83 (a). In response to the objection, applicant notes that "connecting the at least one polysilicon gate to a voltage source for producing latch-up in the multi-region planar thyristor and to a write row address line of a memory integrated circuit, and forming a plurality of channels disposed between the thyristor structures," are shown in at least figures 6, 10, and 1. Figure 6 shows connecting the at least one polysilicon gate to a voltage source for producing latch up in the multi-region planar thyristor. Figure 10 shows connecting the at least one polysilicon gate to a write row address line (34) of a memory integrated circuit. Figure 1 shows forming a plurality of channels disposed between the thyristor structures. Accordingly, the objection to the drawings should be withdrawn.

The specification stands objected to as lacking antecedent basis for the claim terminology "connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor and to a write row address line of a memory integrated circuit," and "forming a plurality of channels disposed between said thyristor structures." Applicant believes that proper antecedent basis for the subject claim language is found in the specification.

In relation to the former limitation the specification discloses "[e]ach bipolar transistor memory cell includes a gate which is pulsed biased during the write operation to latch-up the cell." Column 2, line 53-55. This may be read in light of figure 6, which shows the legend "positive gate voltage" applied to the thyristor gate. The application further states "[w]rite is accomplished by raising the voltage across the cell at the coincidence of the write row address line 34 and column address line 30, to induce carrier multiplication in the gated diode 26. The high voltage induces avalanche breakdown in the gated diode 26, and turns the transistors on strongly. The transistors then latch-up, so that the cell now will be read as storing a "one." The voltage in the write row address line 34 may be immediately lowered once the write operation is completed." Column 6, lines 7-

14. This statement, viewed in the context of figure 10 shows that the specification discloses "connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor and to a write row address line of a memory integrated circuit."

In relation to the latter limitation, figure 1 shows "a plurality of channels disposed between said thyristor structures." This is further supported by the statement in the specification that "[p]lanar transistor pairs or devices, noted generally 12, are separated from each other by isolation trenches 16, 18." Column 4, lines 11-13. Accordingly, proper antecedent basis for the claim language is found in the specification, and the objection to the specification should be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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